## REMARKS

The application contains claims 1 to 29. Claims 1, 8, 11, 17, 22, 23 and 24 are the independent claims. Claims 24-29 are new. In view of the foregoing amendments and following remarks, the Applicants respectfully request allowance of the application.

**The Drawings.**

The Examiner objected to Figure 1 because 'Bus Sequencing Unit 200' is not shown. Figure 1 has been corrected accordingly.

**The Claims Satisfy 35 U.S.C. § 112.**

Both claims 6 and 7 have been amended to depend from claim 5 instead of claim 4. These changes are made merely to correct antecedent basis and are not intended to narrow the scope of the claimed features. Applicants submit that these claims comply with 35 U.S.C. §112.

**The Claims Patentably Define The Invention Over *Sachs*.**

Claims 8-10 and 22 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Sachs, et al., U.S. Patent No. 4,884,197 ("Sachs"). The Applicants respectfully traverse. Claim 8 of the present invention describes a transaction queue having a plurality of queue entries in which a first status portion and a second status portion each correspond to different external transactions relating to the same address. *Sachs* fails to disclose different status portions of an external transaction entry that relate to the same address. *Sachs* instead describes a cache memory storage buffer that contains independent fields W and X, each of which includes its own separate and unique address information. *See, e.g.*, col. 22:49-65. The Applicants respectfully submit that claim 8 is therefore not anticipated by *Sachs* and should be allowed. Claim 22 describes similar subject matter and should be allowed for similar reasons. Finally, the Applicants respectfully submit that dependent claims 9-10 are patentable over *Sachs* for at least the same reasons advanced for claim 8.

**The Claims Patentably Define The Invention Over *Scales*.**

Claims 17-21 and 23 stand rejected under 35 U.S.C. § 102(b) as being anticipated by *Sachs* as well as by Scales, III et al., U.S. Patent No. 4,914,573 ("Scales"). The Applicants re-

spectfully traverse. Neither *Sachs* nor *Scales* teach or suggest certain important features of these claims.

Claim 17 of the present invention describes a method of processing a data request in which a sequence of external transactions are posted to fill a single cache line and where each cache line is sized to store multiple data line lengths of data. As the Examiner admits, *Sachs* does not teach a cache line that is sized to store multiple data line lengths of data. Thus, the Applicants respectfully submit that *Sachs* fails to anticipate claim 17 and 23, as well as claims 18-21, which depend from claim 17.

*Scales* appears to describe a bus master system that responds to a single memory request by automatically supplying additional data in order to fill a cache entry, if necessary. *See, e.g.*, col. 1:37-57. However, *Scales* fails entirely to teach or suggest transferring multiple data line lengths of data whenever a data request misses the cache. A "data line" is well known in the art. It is the maximum amount of data that may be transferred in a single bus transaction, where each bus transaction may require a series of single data transfers on a bus, depending on the particular bus protocol. Embodiments of the present invention sever the one-to-one relationship that existed in the prior art between cache line lengths and data line lengths. Claim 17 focuses on that many-to-one relationship by describing a method of processing data in an agent, in which a sequence of external transactions are posted to fill a cache line "wherein each cache line is sized to store multiple data line lengths of data." Contrary to the Examiner's assertion, *Scales* fails to teach or suggest this many-to-one relationship between a cache line and a data line. In fact, *Scales* fails to discuss a data line transaction at all. Instead, *Scales* is merely concerned with transferring additional operands whenever a requested operand has a size smaller than a single cache entry. *Scales* does not teach or suggest transferring multiple data line lengths of data, as is disclosed by claim 17. Thus, where the present invention posts a sequence of external transactions, each of which transfers a data line length of data, *Scales* responds to a single request for an operand by transferring additional operands back to the agent. *See* col. 2:55-63. Operands, as taught by *Scales* are not data lines, as described by the present invention. For at least this reason, the Applicants respectfully submit that claim 17 is not anticipated by *Scales* and should be allowed. Claim 23 describes similar subject matter and should be allowed for similar reasons. De-

pendent claims 18-21 are patentable over *Scales* for at least the same reasons advanced for claim 17. The Applicants respectfully request that these claims be allowed as well.

**The Claims Patentably Define The Invention Over *Sachs* in view of *Scales*.**

Claims 1-7 and 11-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Sachs* in view of *Scales*. The Applicants respectfully traverse.

Before a claim can be rejected for obviousness under 35 U.S.C. § 103(a), not only must the prior art teach or suggest each element of the claim, the prior art must also suggest combining the elements in the manner contemplated by the claim. *See Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 934 (Fed. Cir. 1990); *In re Bond*, 910 F.2d 831, 834 (Fed. Cir. 1990). The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *See* MPEP § 2142. To satisfy this burden, the Examiner must show, among other things, that there is some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references and that, when so modified or combined, the prior art teaches or suggests all of the claim limitations. *See* MPEP § 2143. The Applicants respectfully submit that neither of these criteria for obviousness have been met here. In the present case, the Examiner has not given any reason to combine *Sachs* with *Scales*, other than "to arrive at Applicant's current invention." *See* Office Action (paper no. 16), p. 7. With regard to the cited references, not only would it be necessary to make modifications, not taught by the prior art, to combine the references in the manner suggested by the Examiner, the references are complete and functional in themselves, and do not suggest modification.

Claim 1 of the present invention describes a processing agent that has an internal cache in which each entry is sized to store multiple data line lengths of data. As the Examiner admits, *Sachs* fails to teach that each cache entry is sized to store multiple data line lengths of data. However, the Examiner suggests that it would have been obvious to one skilled in the art to combine *Sachs* with *Scales* to achieve this feature. As the previous 102(b) discussion makes clear, neither *Sachs* nor *Scales* teach or suggest a cache entry sized to store multiple data line lengths of data. Thus, the Applicants respectfully assert that even if *Scales* were combined with *Sachs* in the manner suggested by the Examiner, all the features of claim 1 would still not be achieved.

The Applicants respectfully submit that claim 1 patentably defines the invention over *Sachs* in view of *Scales*. For the same reasons, the Applicants suggest that independent claim 11, as well as dependent claims 1-4, 6-7 and 12-16, which depend from claims 1 and 11, also are patentable over *Sachs* in view of *Scales*.

**New Claims are Patentable Over the Cited References.**

New claim 24 describes a processing agent having a plurality of cache entries, where each cache entry is sized to store one data line length of data, and where each external transaction is related to the same address information. For the reasons outline above for claims 8 and 17, the Applicants respectfully submit that claim 24 is patentable over *Sachs* and/or *Scales* and should be allowed.

Dependent claims 25-29 each recite that a "data line" corresponds to the maximum amount of data that can be transferred in a single bus transaction. This merely makes explicit in a dependent claim what is implied in the corresponding independent claims. As noted, neither *Sachs* nor *Scales* teaches or suggests a cache entry that is sized to store multiple *data line* lengths of data. Thus, the Applicants respectfully assert that claims 25-29 are patentable over the cited references and should be allowed.

**Conclusion**

In view of the above amendments and remarks, the Applicants respectfully submit that the present application is now in condition for allowance. A Notice to that effect is earnestly solicited. The Examiner is invited to contact the undersigned at (202) 220-4200 to discuss any aspect of the application.

Respectfully submitted,

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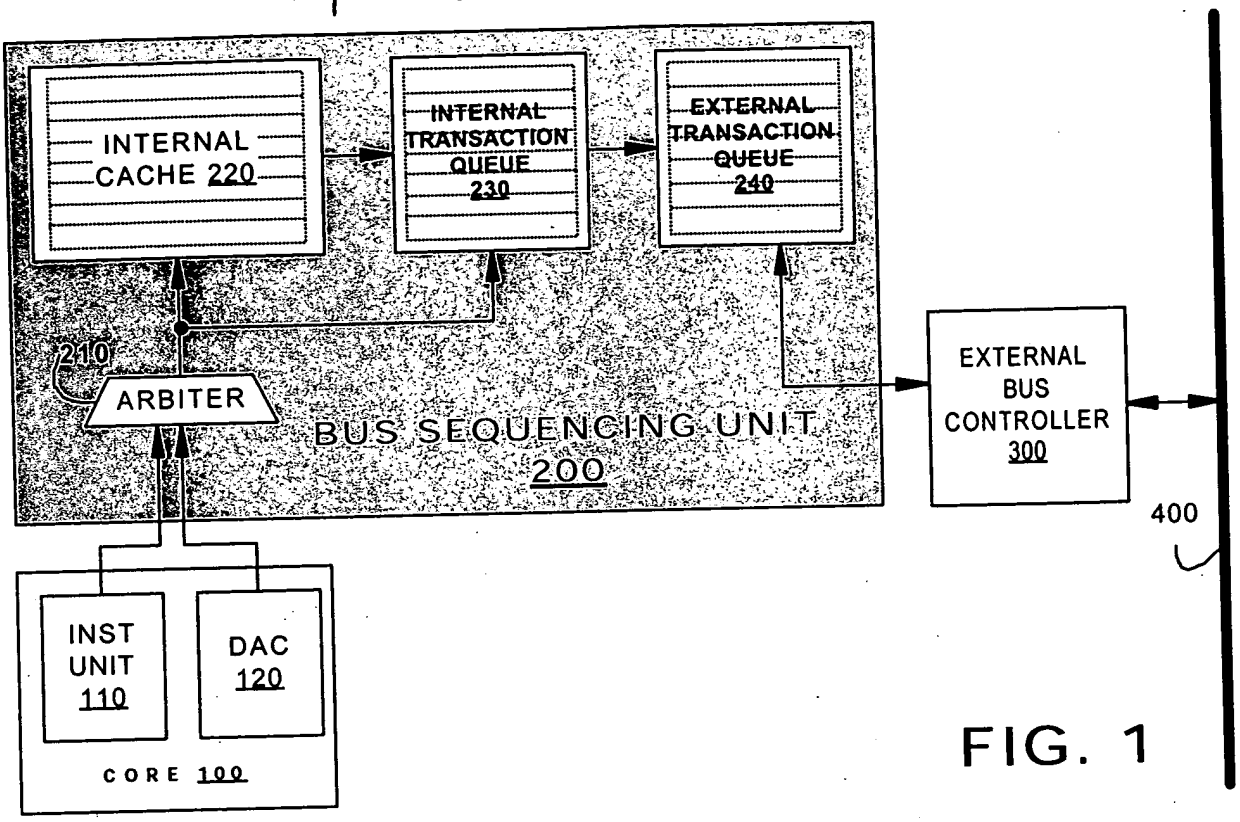


FIG. 1

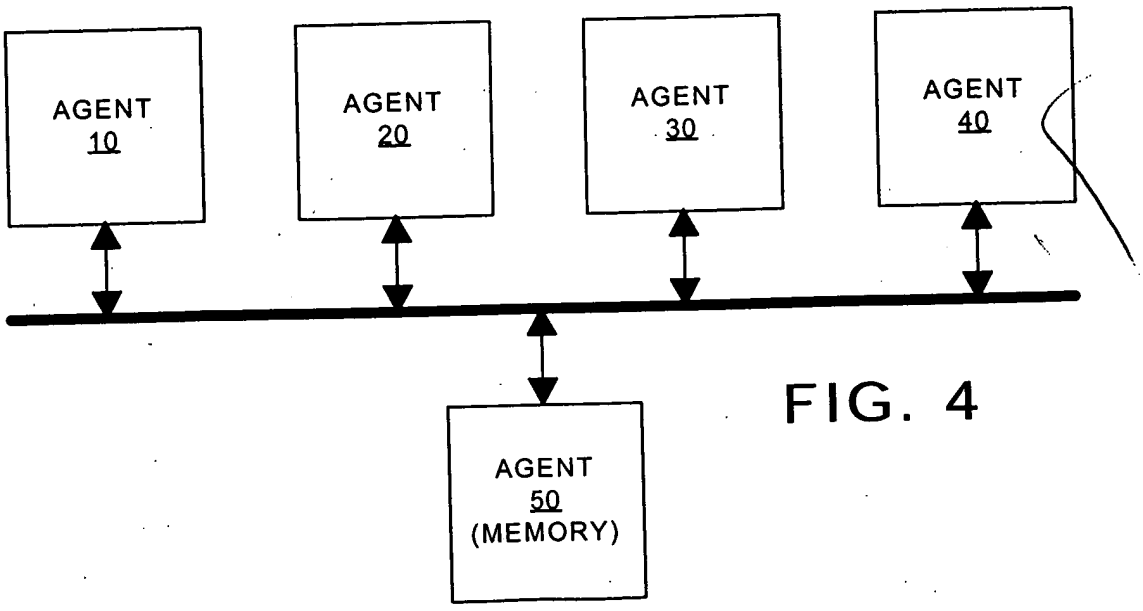


FIG. 4